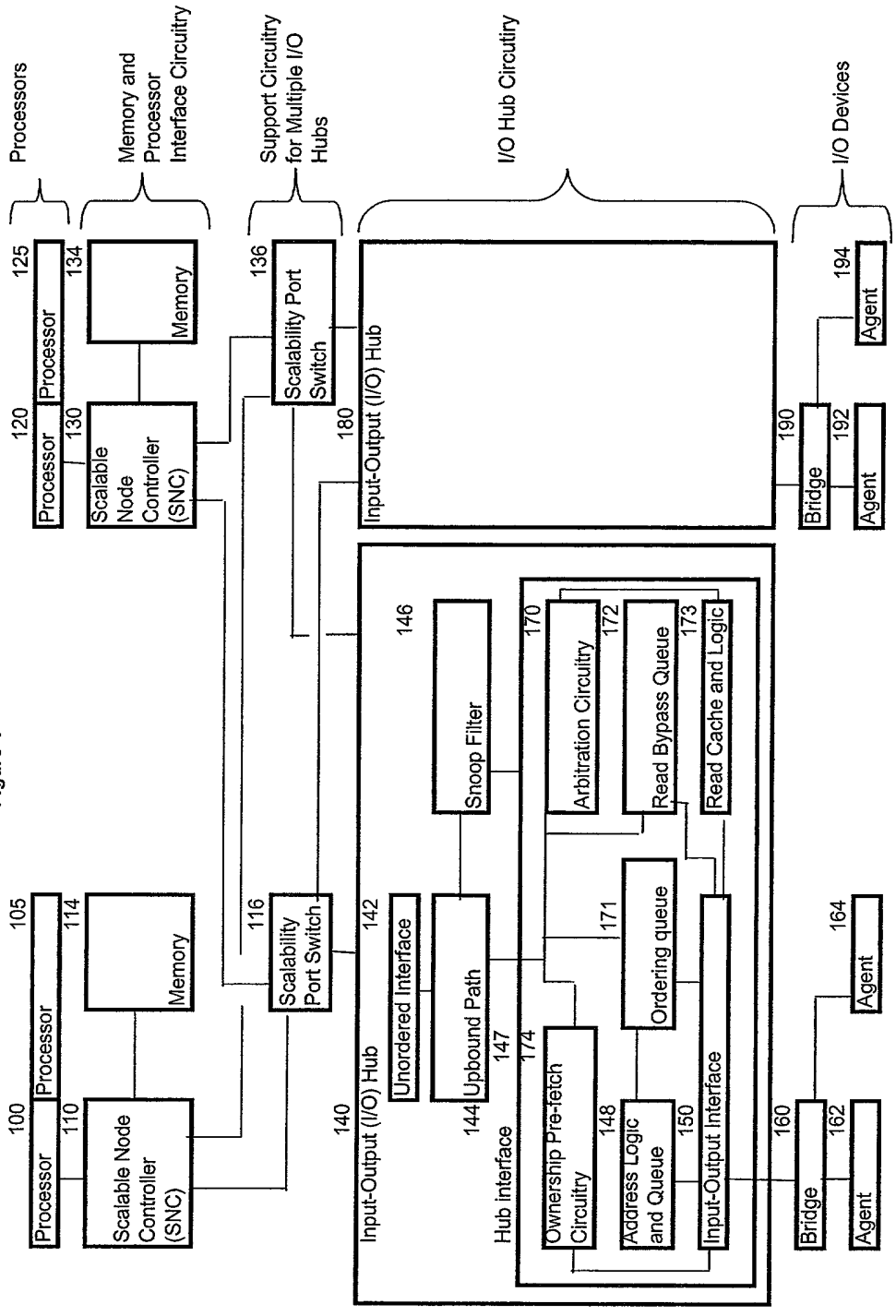

Processors
Memory and Processor Interface Circuitry
Support Circuitry for Multiple I/O Hubs
I/O Hub Circuitry
I/O Devices
Processor
Scalable Node Controller (SNC)
Memory
Scalability Port Switch
Input-Output (I/O) Hub
Bridge
Agent
Unordered Interface
Upbound Path
Hub interface
Snoop Filter
Arbitration Circuitry
Read Bypass Queue
Read Cache and Logic
Ordering queue
Ownership Pre-fetch Circuitry
Address Logic and Queue
Input-Output Interface

Figure 1

Figure 2

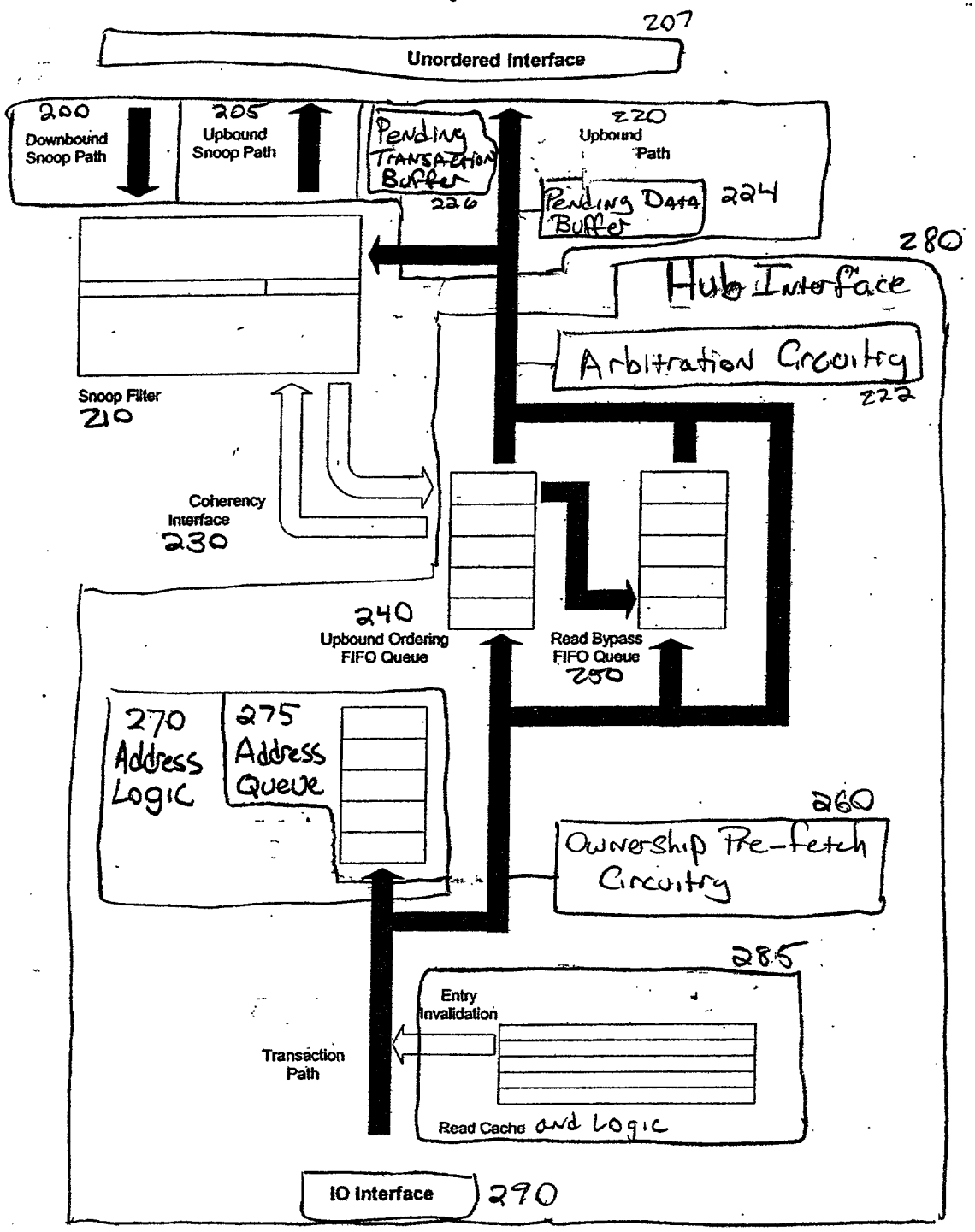
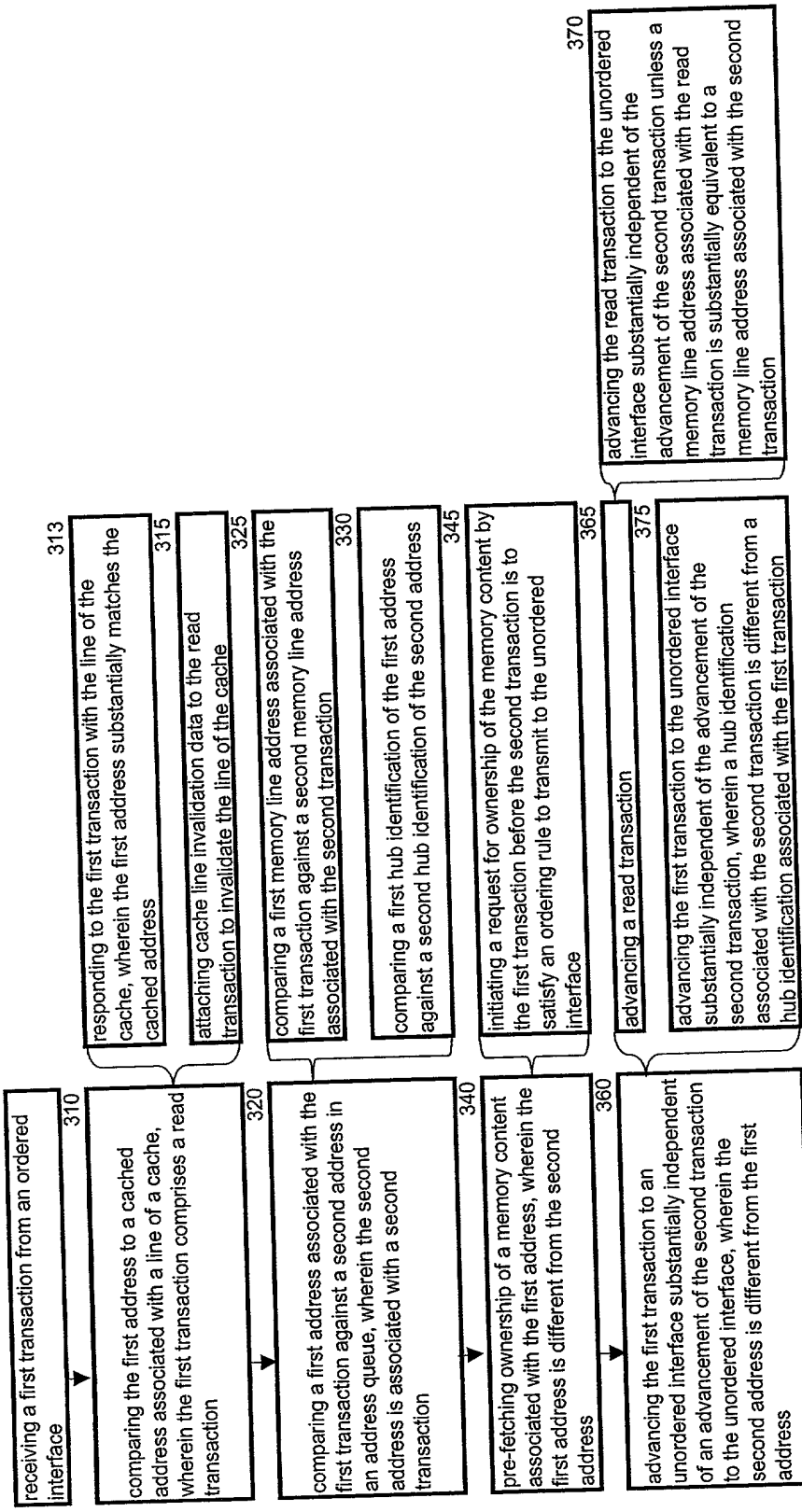

207
Unordered Interface
200
Downbound Snoop Path
205
Upbound Snoop Path
Pending Transaction Buffer
226
220
Upbound Path
Pending Data Buffer
224
280
Hub Interface
Arbitration Circuitry
222
Snoop Filter
210
Coherency Interface
230
240
Upbound Ordering FIFO Queue
Read Bypass FIFO Queue
250
270
Address Logic
275
Address Queue
260
Ownership Pre-fetch Circuitry
285
Entry Invalidation
Transaction Path
Read Cache and Logic
IO Interface
290

Figure 3


300
receiving a first transaction from an ordered interface
310
comparing the first address to a cached address associated with a line of a cache, wherein the first transaction comprises a read transaction
313
responding to the first transaction with the line of the cache, wherein the first address substantially matches the cached address
315
attaching cache line invalidation data to the read transaction to invalidate the line of the cache
325
320
comparing a first address associated with the first transaction against a second address in an address queue, wherein the second address is associated with a second transaction
comparing a first memory line address associated with the first transaction against a second memory line address associated with the second transaction
330
comparing a first hub identification of the first address against a second hub identification of the second address
345
340
pre-fetching ownership of a memory content associated with the first address, wherein the first address is different from the second address
initiating a request for ownership of the memory content by the first transaction before the second transaction is to satisfy an ordering rule to transmit to the unordered interface
365
360
advancing the first transaction to an unordered interface substantially independent of an advancement of the second transaction to the unordered interface, wherein the second address is different from the first address
advancing a read transaction
375
advancing the first transaction to the unordered interface substantially independent of the advancement of the second transaction, wherein a hub identification associated with the second transaction is different from a hub identification associated with the first transaction
370
advancing the read transaction to the unordered interface substantially independent of the advancement of the second transaction unless a memory line address associated with the read transaction is substantially equivalent to a memory line address associated with the second transaction

Attorney Docket

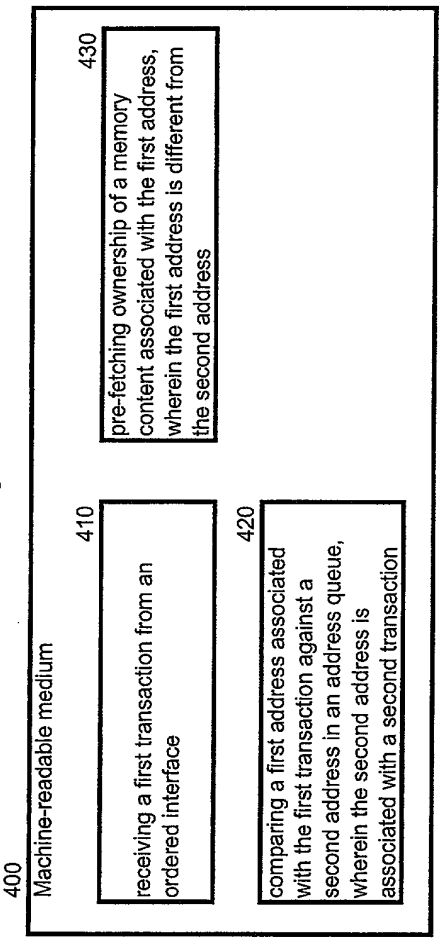



Figure 4